iSim™ ISL6742 Virtual Evaluation Platform

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Introduction

Intersil's iSim™ is an interactive, web-based tool for selecting and simulating products and their applications from Intersil's broad portfolio. Currently, iSim™ is available for Intersil's power management devices and operational amplifiers.

The iSim™ simulation tool excels at simulating moderate time scale behavior which is required for simulations of power supplies during steady state and transient operation. It runs quickly compared to other simulation tools by using simplified device models and by detecting switching transitions and adjusting step size accordingly to achieve the required accuracy. Detailed device behavior is not modeled as accurately as tools like PSPICE™ so that simulation time can be minimized. This results in overall switching, and small and large signal behavior being faithfully modeled while fast transitions and detailed device behavior are simplified. For further details on iSim, please consult the Intersil web site at http://www.intersil.com/isim/.

The ISL6742 is a high-performance double-ended PWM controller with advanced synchronous rectifier control and current limit features. It is suitable for both current- and voltage-mode control methods. It includes complemented PWM outputs for synchronous rectifier (SR) control. The complemented outputs may be dynamically advanced or delayed relative to the main outputs using an external control voltage.

Its advanced current sensing circuitry employs sample and hold methods to provide a precise average current signal. Suitable for average current limiting, a technique which virtually eliminates the current tail-out common to peak current limiting methods, it is also applicable to current sharing circuits and average current control.

All these features are packaged in a 16 Lead QSOP. A more complete description of the IC can be found in the datasheet[1].

The simulation topology supported by iSim™ is a hard-switched full-bridge voltage-mode current-doubler configuration. The default settings are for a 48V to 3.3V converter rated at 75A. All component values plus the input and output voltages may be changed by the user. Component interconnections can not be modified.

Getting Started

The ISL6742 iSim™ schematic may be accessed from the Intersil web site at http://www.intersil.com/isim/isimpower.asp. It may be necessary to adjust your web browser settings. Please refer to the web page link to application note AN1191.

Scroll/page down under the section *Switching Regulation* and locate the link to the ISL6742. Left click the icon. If you are a new user of iSim, It will be necessary to register. Otherwise you may need to login. Once successfully logged-in, the ISL6742 iSim™ simulation page loads with the *Analyze* tab pre-selected. The *Analyze* tab includes the simulation schematic and menu/execution options. The schematic has labeled current and voltage probe points to identify viewable waveforms. The probe points are fixed and can not be moved. Changeable parameters are identified in blue type. Select the device (not the parameters) to make changes. Some component values will update automatically when other components are changed. Changes that affect the proper operation of the power supply will automatically cause critical component values to be re-calculated. Changing the value of the output inductor, for example, will cause the control loop compensation to be re-calculated. Any calculated value can be over-ridden by manually adjusting that value. Once a value has been manually changed, the component value will no longer be updated automatically. For the remainder of the current design session, the component value can only be changed manually. To change back to automatic re-calculate mode, the reference design schematic must be re-loaded. All manual updates will be lost.

Familiarize yourself with the instructions at the top of the iSim™ ISL6742 simulation web page.

Directly above the simulation schematic are menu selections for simulation type, simulation configuration, simulation execution, waveform viewing, and other features. See Figure 1.

The *Select Simulation* tab allows the user to select from three simulation options: small signal AC, steady state, and transient operation. Depending on the simulation selected, the Configuration tab label changes to *Configure AC Analysis*, *Configure Steady State*, or *Configure Transient Analysis*. The Configuration tab is used to set simulation options. For AC analysis, the user may select the frequency range. For transient analysis, the user may select the time span to be simulated. For steady state operation there are no configuration options.

Once a simulation has been selected and configured, select the *Run* tab to begin execution. The Run tab label changes, depending on the simulation selected, to *Run AC Analysis*, *Run Steady State*, or *Run Transient Analysis*. The simulation takes several minutes to run. Once the simulation is completed, the results may be viewed with the *View Waveforms* tab. The waveforms are categorized into related groupings to facilitate locating them.

The *Update Schematic* tab is only required if the schematic has been updated without a subsequent simulation run. Updating the schematic updates the parts list (BOM) as well. It is important to update the schematic if you are saving designs for future use.

Modified schematics and BOMs may be saved using the *My Designs* tab. Designs may be saved and retrieved using this feature.

The *Input Requirements* and *Solutions* tabs may be used to select other Intersil parts and applications. They should not be invoked if the ISL6742 is the desired part.

If an extended period of time elapses without activity, the simulation window becomes invalid. The simulation may appear to run, but new waveforms will not be available and the simulation run time will be very short. The application must be reloaded to continue. All material that was not saved will have been lost.

AC Analysis

The AC Analysis simulation option generates a Bode plot of the converter loop. Loop bandwidth, phase and gain margins are easily determined for the converter.

Select *AC Analysis* from the *Select Simulation* menu button.

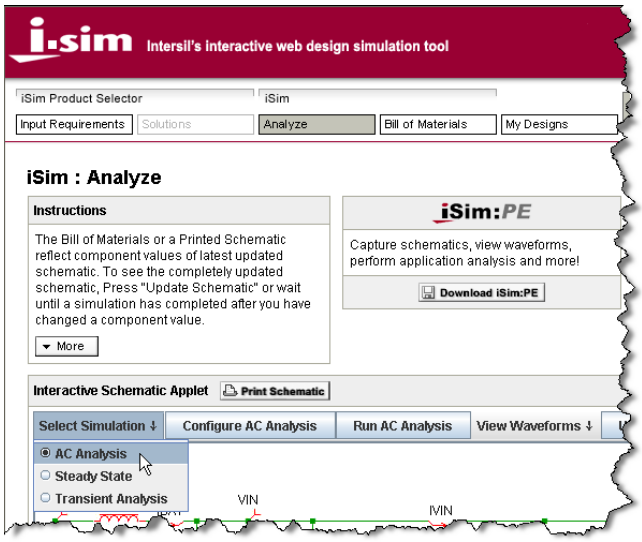


FIGURE 1. *ANALYZE* MENU BUTTONS

Using the *Configure AC Analysis* menu, change the frequency range for the Bode plot as desired, or leave the default values intact. Start the analysis using the *Run AC Analysis* button. The results may be viewed from the *View Waveforms* menu. The resulting Bode plot using the default schematic values appears in Figure 2.

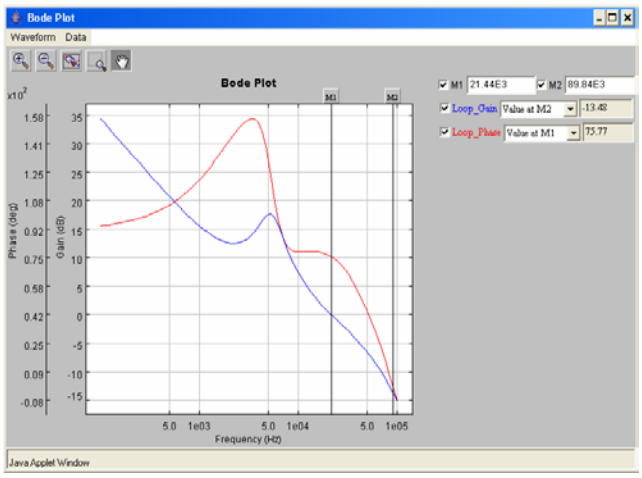


FIGURE 2. BODE PLOT

Two vertical cursors, M1 and M2, are available to measure gain or phase margin at a selected frequency. They may be invoked by selecting the appropriate box located in the legend at the upper right of the graph. Likewise, the gain and phase margin plots may be turned on and off using the box located immediately to the left of the corresponding label in the legend.

The displays to the right of the M1/M2 labels indicate the x-axis value (frequency) of the vertical cursor it corresponds to. The display contents for gain and phase margin may be selected using the drop down menu immediately to the right of the label.

Waveform windows may be captured for pasting into other documents by using the *alt-Print Screen* on the keyboard. The results will be contained in the clipboard.

In this example, the loop has a bandwidth of 21.44kHz, a phase margin of 75.77°, and a gain margin of -13.48dB.

Steady State Analysis

The Steady State Analysis simulation option generates a complete set of steady state operating waveforms.These are particularly useful for understanding the basic operation of the ISL6742 and the converter, particularly the timing and tuning of the synchronous rectifiers (SRs).

Select *Steady State* from the *Select Simulation* menu tab. Start the analysis using the *Run Steady State* button. The resulting waveforms are can be viewed using the *View Waveforms* button when the simulation is finished. The waveforms are categorized into several groups. Select the waveform group to be observed. Multiple waveform windows may be opened and observed simultaneously.

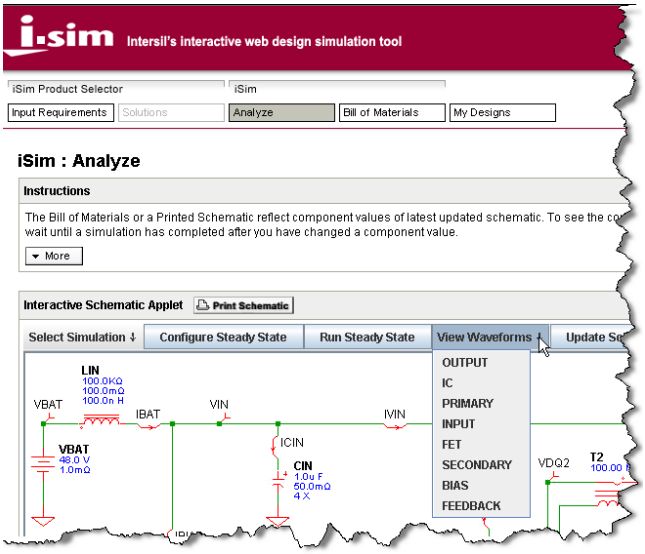


FIGURE 3. *VIEW WAVEFORMS* TAB PULL-DOWN

Selecting one of the categories of waveforms from the list loads those waveforms into a viewing window. It will take several moments for the data to download. An example of the *FET* waveforms appears below:

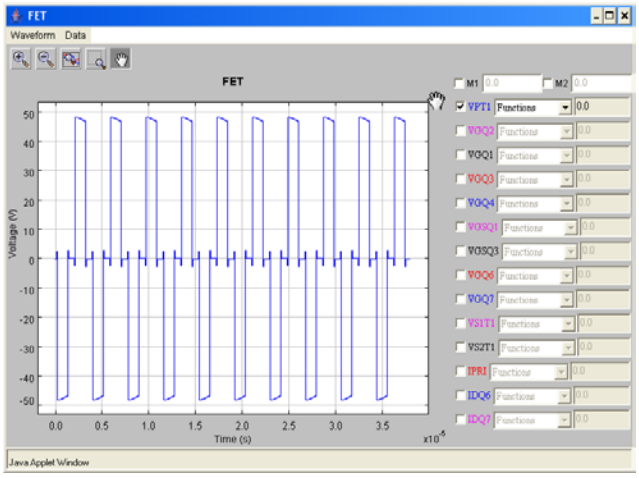


FIGURE 4. EXAMPLE OF VIEWABLE WAVEFORMS

Left-clicking the box adjacent to the waveform name causes that waveform to be displayed. The cursors, M1 and M2, are available to measure amplitude at any point on the time axis. They may be invoked by selecting the appropriate box located in the legend at the upper right of the graph. The time location of the cursor is displayed in the box immediately adjacent to the cursor label. The amplitude value at the cursor location may be selected using the pull-down menu to the right of the waveform name. RMS and average waveform values are also available.

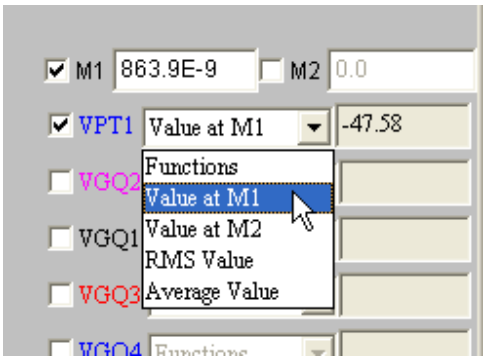


FIGURE 5. WAVEFORM MEASUREMENT OPTIONS

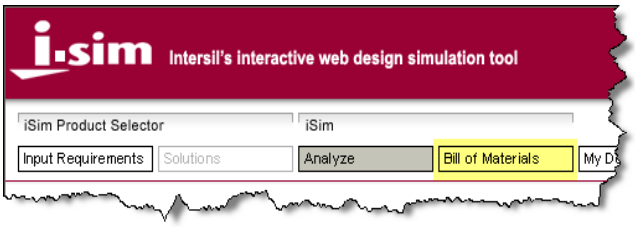


FIGURE 6. *BILL OF MATERIALS* TAB LOCATION

A Bill of Materials (BOM) of the design can be generated at any time using the *Bill of Materials* button located in the upper left section of the page. If component values have been modified without executing a simulation, the component database must be updated first using the *Update Schematic* button, located just above the schematic.

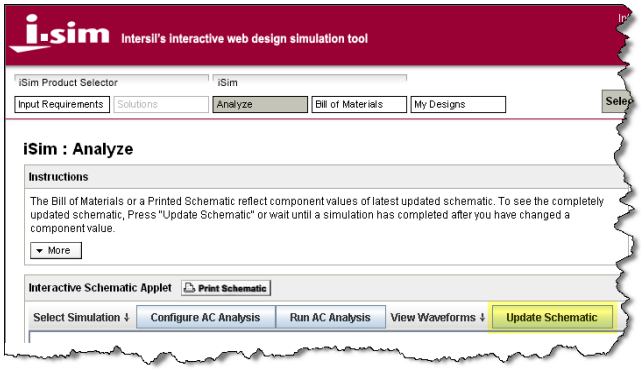


FIGURE 7. *UPDATE SCHEMATIC* TAB LOCATION

An example BOM can be found on page 8.

The steady state analysis is useful for exploring the special features of the ISL6742, particularly the synchronous rectifier timing. The simulation schematic allows the designer to adjust the propagation delays of the FET driver ICs and to correct for differences in the delays between the primary and secondary control signals using the VADJ pin of the ISL6742. The FET driver propagation delay may be adjusted by left-clicking the FET driver schematic symbol. Figure 8

depicts the default SR timing using the drain-source voltage waveforms of Q6.

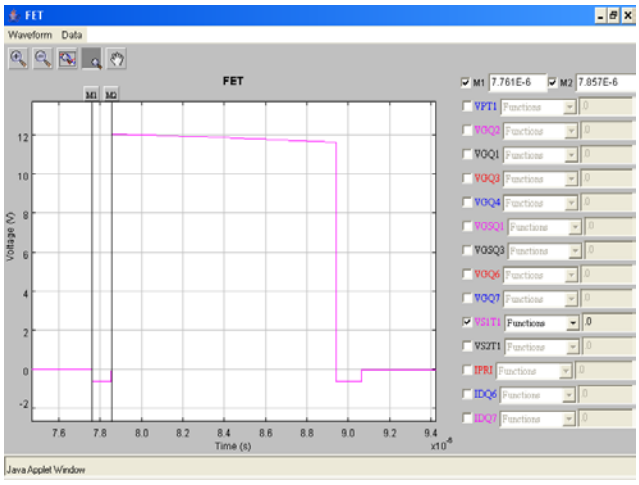


FIGURE 8. SR FET Q6 DRAIN-SOURCE VOLTAGE. TURN-ON NON-OVERLAP TIMING IS INDICATED BY M2-M1.

Although the primary side FET drivers are specified, the SR FET drivers are generic and have additional parameters available for adjustment. In particular, the r_{DSON} and maximum drive current of the driver are adjustable. This allows the designer to match the drive capability to the requirements of the application.

Transient Analysis

The Transient Analysis option allows the user to view the behavior of the power supply during a step load change to the converter output.

A Transient analysis is configured and executed much the same as the Steady State analysis. From the *Select Simulation* pull-down menu, select *Transient Analysis*. Adjust the duration of the simulated operation as desired from the *Configure Transient Analysis* tab. Selecting longer periods of operation will result in longer run times. Simulation times on the order of several minutes per 100µs of operation can be expected. As before, the resulting waveforms can be viewed using the *View Waveforms* button when the simulation is finished.

Figure 9 shows the output voltage deviation caused by a 30A to 60A step load with a 100ns risetime on a 3.3V, 75A converter.

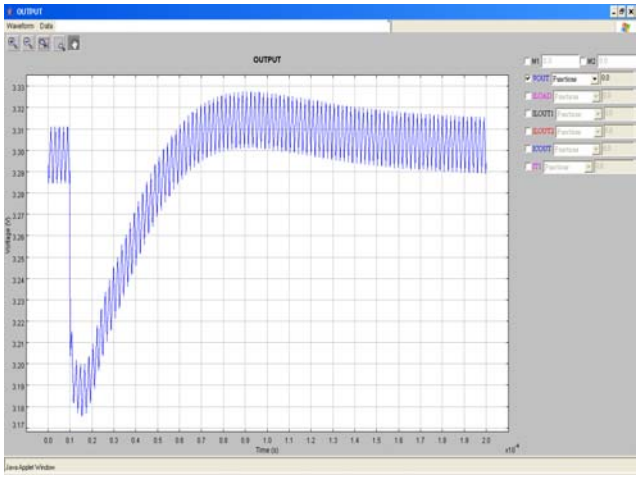


FIGURE 9. TRANSIENT ANALYSIS RESULTS FOR A 30A-60A OUTPUT STEP LOAD

The transient analysis is useful for exploring the average current limit feature of the ISL6742. Figures 10 and 11 show the response of the current sense signal at CS and the resulting signal at IOUT. The average current for each inductor is captured by the sample and hold circuit on alternate half-cycles.

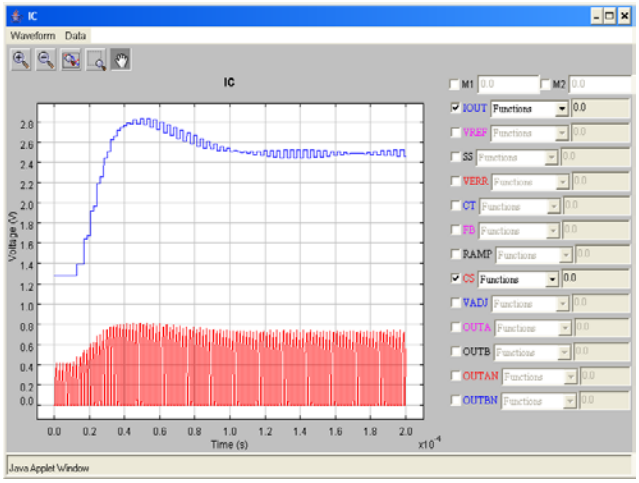


FIGURE 10. CURRENT SENSE (CS) INPUT AND AVERAGE CURRENT (IOUT) SIGNAL WAVEFORMS RESULTING FROM AN OUTPUT STEP LOAD

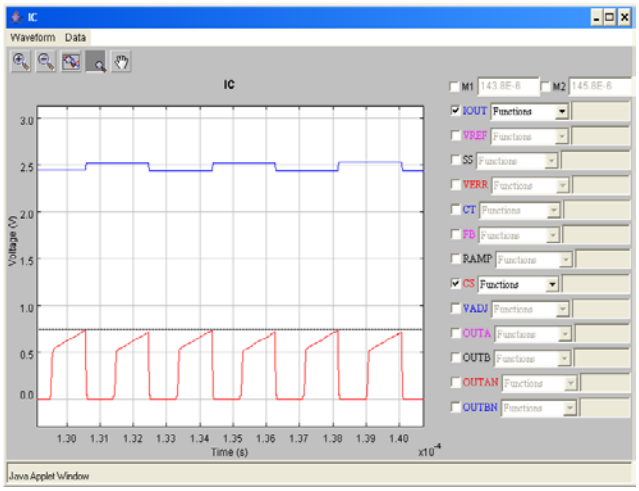


FIGURE 11. EXPANDED WAVEFORMS FROM FIGURE 10. NOTE THE SLIGHT DIFFERENCE IN AMPLITUDE OF THE ALTERNATE HALF-CYCLE CURRENT SENSE WAVEFORM.

Remembering the current-doubler output topology and that voltage-mode control is used, the stepped behavior of IOUT reflects the oscillation of the current in the output inductors due to the LC resonant tank formed by the DC blocking capacitor and the effective inductance in the primary. The output step load disturbs the tank circuit resulting in a damped oscillation. See Figure 12.

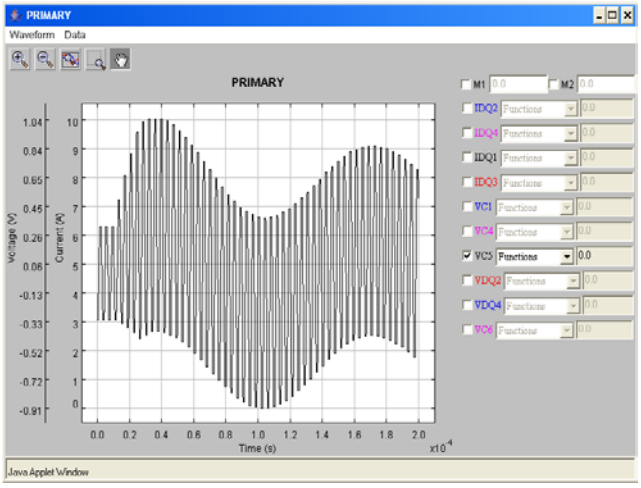


FIGURE 12. VOLTAGE WAVEFORM ACROSS THE DC BLOCKING CAPACITOR C5

The average current limit circuit not only results in a very uniform current limit, but also corrects for the flux imbalance that occurs when peak current limit is used in voltage-mode controlled power supplies. The average current limit signal, IOUT, is integrated against a reference and the resulting signal modulates the error voltage, VERR. See Figure 14. Figure 13 shows the output response when the converter is placed in extended current limit. The response time of the average current limit circuit is user adjustable. In this example, C11 and R12 were set to 220pF and 100Ω, respectively, to shorten the simulation time. Like any closed loop feedback system, the average current limit circuit requires proper compensation to prevent oscillation.

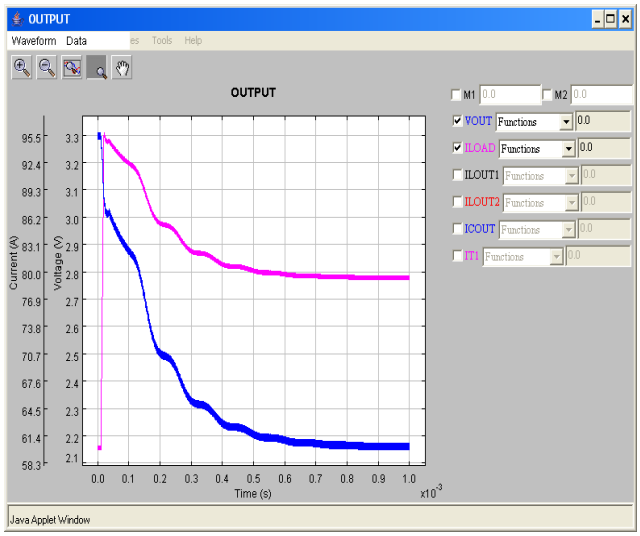


FIGURE 13.

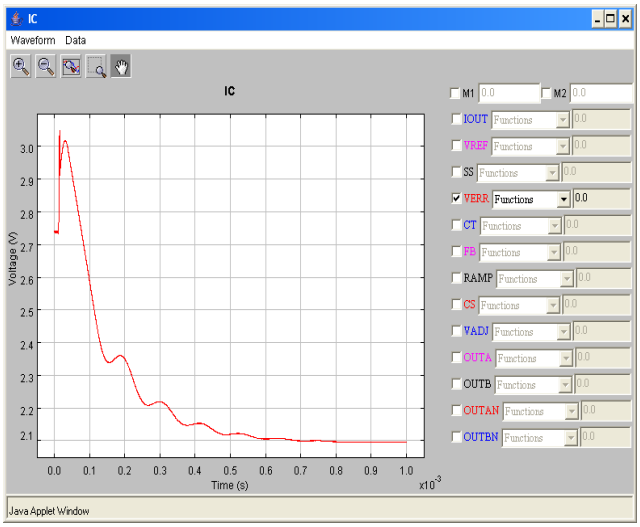


FIGURE 14. VERR MODULATED BY THE AVERAGE CURRENT AMPLIFIER IN RESPONSE TO AN EXTENDED CURRENT LIMIT

When a step load exceeding the current limit setpoint is applied to the output of the power supply, several events occur. First, the peak current limit protects the power supply on a cycle-by-cycle basis until the average current limit circuit responds. Using peak current limit will cause a volt-second imbalance because the DC blocking capacitor charge is now controlled by the peak current limit rather than the volt-seconds across the transformer primary. This results in a net charge building up on the DC blocking capacitor and the bridge becomes unbalanced. The peak current limit

starts to trip on one half-cycle only. If left unchecked, the DC blocking capacitor would eventually charge up to the supply rail.

The average current limit circuit prevents this behavior by forcing the same duty cycle on both half-cycles. Figure 15 shows the response of CS and IOUT to a step load into current limit. Initially CS is clipped at the 1 V peak current limit setpoint before the average current circuit limit responds. The average current limit circuits requires some time to damp oscillation on the DC blocking capacitor.

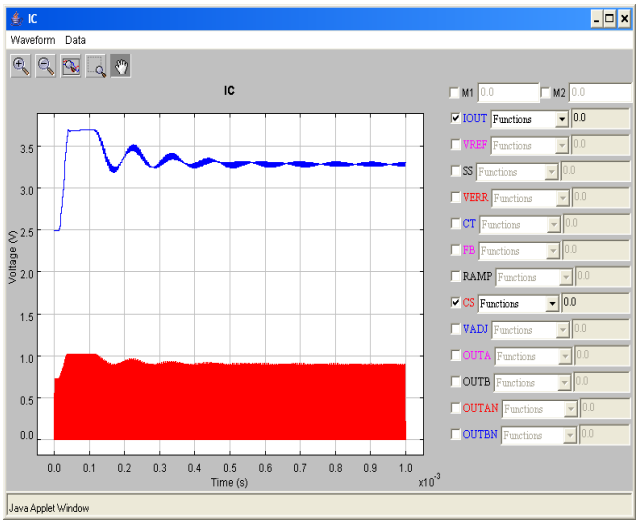


FIGURE 15. IOUT AND CS RESULTING FROM A STEP LOAD INTO CURRENT LIMIT

Conclusion

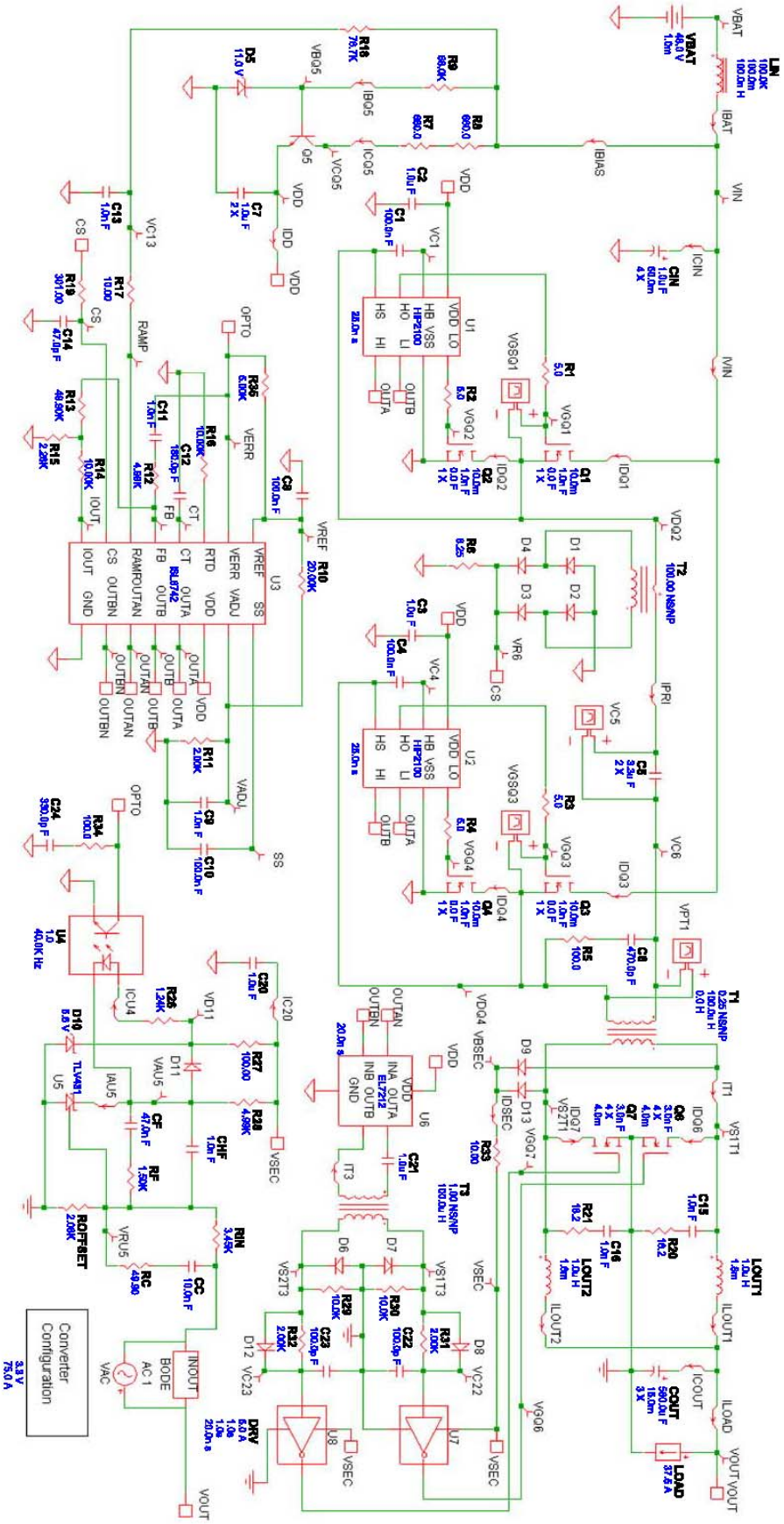
The ISL6742 iSim™ simulation tool provides the designer with a virtual test platform. More than just an educational tool, it allows the prospective designer to evaluate nearly all of the design decisions prior to committing resources to a physical realization.

References

For Intersil documents available on the web, see http://www.intersil.com/

[1] *ISL6742 Data Sheet,* Intersil Corporation, File No. FN9183.

ISL6742 iSim™ Simulation Schematic



ISL6742 Sample Bill of Materials (Default Values)

REF	# OF PARTS	VALUE	DESCRIPTION
U1	1	HIP2100	IC
U2	1	HIP2100	IC
U3	1	ISL6742	IC
U4	1		Opto
U5	1	TLV431	IC
U6	1	EL7212	IC
U7	1		Generic Driver
U8	1		Generic Driver
C1	1	100.0n F	Capacitor
C2	1	1.0u F	Capacitor
C3	1	1.0u F	Capacitor
C4	1	100.0n F	Capacitor
C5	2	3.3u F	Capacitor
C6	1	470.0p F	Capacitor
C7	2	1.0u F	Capacitor
C8	1	100.0n F	Capacitor
C9	1	1.0n F	Capacitor
C10	1	100.0n F	Capacitor
C11	1	1.0n F	Capacitor
C12	1	180.0p F	Capacitor
C13	1	1.0n F	Capacitor
C14	1	47.0p F	Capacitor
C15	1	1.0n F	Capacitor
C16	1	1.0n F	Capacitor
C20	1	1.0u F	Capacitor
C21	1	1.0u F	Capacitor
C22	1	100.0p F	Capacitor
C23	1	100.0p F	Capacitor
C24	1	330.0p F	Capacitor
CC	1	10.0n F	Capacitor
CF	1	47.0n F	Capacitor
CHF	1	1.0n F	Capacitor
CIN	4	1.0u F	Capacitor
COUT	3	560.0u F	Capacitor
D1	1	BAT54S	Diode
D2	1	BAT54S	Diode
D3	1	BAT54S	Diode
D4	1	BAT54S	Diode
D5	1	11.0 V	Zener Diode
D6	1	BAT54S	Diode
D7	1	BAT54S	Diode
D8	1	BAT54S	Diode
D9	1	BAT54S	Diode
D10	1	5.6 V	Zener Diode
D12	1	BAT54S	Diode
D13	1	BAT54S	Diode
LIN	1	100.0n H	Inductor
LOUT1	1	1.0u H	Inductor
LOUT2	1	1.0u H	Inductor
Q1	1	10.0m Ohm / 72.0 V	MOSFET
Q2	1	10.0m Ohm / 72.0 V	MOSFET
Q3	1	10.0m Ohm / 72.0 V	MOSFET
Q4	1	10.0m Ohm / 72.0 V	MOSFET
Q6	4	4.0m Ohm / 3.3 V	MOSFET
Q7	4	4.0m Ohm / 3.3 V	MOSFET
R1	1	5.0 Ohm	Resistor
R2	1	5.0 Ohm	Resistor
R3	1	5.0 Ohm	Resistor
R4	1	5.0 Ohm	Resistor
R5	1	100.0 Ohm	Resistor
R6	1	8.25 Ohm	Resistor
R7	1	680.0 Ohm	Resistor
R8	1	680.0 Ohm	Resistor
R9	1	68.0K Ohm	Resistor
R10	1	20.00K Ohm	Resistor
R11	1	2.00K Ohm	Resistor
R12	1	4.99K Ohm	Resistor
R13	1	49.90K Ohm	Resistor
R14	1	10.00K Ohm	Resistor
R15	1	2.26K Ohm	Resistor
R16	1	10.00K Ohm	Resistor
R17	1	10.00 Ohm	Resistor
R18	1	78.7K Ohm	Resistor
R19	1	301.00 Ohm	Resistor
R20	1	18.2 Ohm	Resistor
R21	1	18.2 Ohm	Resistor
R26	1	1.24K Ohm	Resistor
R27	1	100.00 Ohm	Resistor
R28	1	4.99K Ohm	Resistor
R29	1	10.0K Ohm	Resistor
R30	1	10.0K Ohm	Resistor
R31	1	2.00K Ohm	Resistor
R32	1	2.00K Ohm	Resistor
R33	1	10.00 Ohm	Resistor
R34	1	100.0 Ohm	Resistor
R35	1	5.00K Ohm	Resistor
RC	1	49.90 Ohm	Resistor
RF	1	1.50K Ohm	Resistor
RIN	1	3.45K Ohm	Resistor
ROFFSET	1	2.08K Ohm	Resistor
T1	1	Lkg. Ind. 0.0 H / Mag. Ind. 100.0u H Turns Ratio 0.25	Transformer
T2	1	Turns Ratio 0.01	Current Sense Transformer
T3	1	100.0u H Turns Ratio 1.00	Transformer